WHAT IS CLAIMED IS:

1. A method of forming a circuit element on a semiconductor wafer comprising:

forming a dielectric layer on a semiconductor wafer;

forming a shield layer on the dielectric layer;

forming a first cavity in the dielectric layer;

depositing conductive material on the wafer so that the conductive material coats the exposed surfaces of the first cavity and so that the conductive material does not completely fill the cavity so as to define a second cavity within the first cavity;

removing the excess conductive material by chemical mechanical polishing (CMP), wherein the shield layer inhibits thinning of the dielectric layer during the chemical mechanical polishing.

2. The method of Claim 1, wherein forming the shield layer comprises forming an antireflective coating.

3. The method of Claim 2, wherein forming an antireflective coating comprises forming a dielectric antireflective layer.

4. The method of Claim 1, wherein forming the shield layer comprises forming a CMP resistant shield layer.

5. The method of Claim 4, wherein forming a shield layer comprises forming a Silicon Nitride layer.

6. The method of Claim 1, wherein removing the excess conductive material by chemical mechanical polishing (CMP) comprises:

positioning the semiconductor wafer adjacent a polishing pad of a CMP system in a flush manner;

interposing a slurry material between the semiconductor wafer and the polishing pad; and

displacing the semiconductor wafer with respect to the polishing pad so that frictional engagement therebetween removes excess conductive material from the semiconductor wafer; and

detecting an end point which indicates that the excess conductive material has been removed by the CMP system.

7. The method of Claim 6, wherein detecting an end point comprises monitoring the torque exerted by the polishing pad onto the semiconductor wafer and assigning the occurrence of the end point to a relatively large increase in the monitored torque.

8. The method of Claim 7, wherein monitoring the torque exerted by the polishing pad comprises monitoring the current used by the CMP system.

9. The method of Claim 6, wherein detecting an end point comprises:

directing a beam of light toward an exposed surface of the semiconductor wafer;

monitoring the amount of light reflected off of the semiconductor wafer; and

assigning the occurrence of the end point to a relatively large decrease in the monitored light.

10. The method of Claim 1, further comprising:

depositing fill material above the conducting material so that the fill material substantially fills in the second cavity;

subsequent to depositing the fill material, removing the excess fill material using CMP so that the second cavity remains substantially filled in by the fill material so as to maintain the integrity of the remaining conductive material;

removing the remaining fill material subsequent to CMP so as to redefine the second cavity;

11. The method of Claim 10, wherein depositing fill material above the conducting material comprises depositing photoresist material above the conductive material.

12. The method of Claim 11, wherein removing the remaining fill material comprises exposing the remaining fill material to an oxidizing etchant.

13. The method of Claim 1, further comprising forming a sacrificial layer on the shield layer so that the sacrificial layer is interposed between the excess conductive material and the shield layer.

14. The method of Claim 13, wherein the sacrificial layer is comprised of a BPSG Oxide layer of 200 - 1,000 Angstroms thickness.

15. The method of Claim 14, wherein the removal of the excess conductive material comprises using CMP to remove both the excess conductive material and the sacrificial layer.

16. The method of Claim 1, wherein forming a cavity in the dielectric layer comprises forming a trench in the dielectric layer.

17. A method of forming a conductive element in a dielectric layer on a semiconductor wafer comprising:

positioning a shield layer on the dielectric layer;

positioning a sacrificial layer on the shield layer;

forming a cavity in the dielectric layer;

depositing conductive material on the sacrificial layer so that the conductive layer is positioned within the cavity;

using chemical mechanical polishing (CMP) to remove the excess conductive material and the sacrificial layer, wherein the CMP is performed using an etchant selected to remove the sacrificial layer and wherein the shield layer is resistant to the selected etchant.

18. The method of Claim 17, wherein the shield layer is comprised of a Nitride layer positioned on the dielectric layer.

19. The method of Claim 18, wherein the sacrificial layer is comprised of a BPSG Oxide layer formed on the Nitride layer and the conductive material is comprised of Polysilicon.

20. The method of Claim 17, wherein detecting the end point comprises sensing the current being drawn by a motor inducing relative movement between a polishing pad and the wafer and sensing when the current drawn by the motor indicates that the pad is in contact with the shield layer.

21. The method of Claim 20, wherein frictional forces between a polishing pad containing the slurry and the surface of the wafer being planarized increases as a result of removal of the sacrificial layer due to the relative imperviousness of the shield layer to the etchant of the slurry.

22. The method of Claim 17, wherein the shield layer is comprised of an antireflective layer positioned on the dielectric layer.

23. The method of Claim 22, wherein the antireflective layer comprises a dielectric antireflective coating comprising Silicon, Oxygen and Nitrogen.

24. The method of Claim 23, wherein the sacrificial layer is comprised of a BPSG Oxide layer formed on the DARC Oxide layer and the conductive material is comprised of Polysilicon.

25. The method of Claim 17, further comprising detecting an end point indicative of the removal of the sacrificial layer.

26. The method of Claim 25, wherein detecting the end point comprises directing a beam of light onto the surface of the wafer, sensing the light reflected from the wafer, and sensing when the light reflected from the wafer indicates that the pad is in contact with the shield layer.

27. The method of Claim 26, wherein the amount of light reflected from the wafer decreases as a result of removal of the sacrificial layer due to the relatively low reflectivity of the shield layer.

28. The method of Claim 17, wherein forming a cavity in the dielectric layer comprises forming a trench in the dielectric layer.

29. The method of Claim 28, wherein depositing conductive material on the sacrificial layer comprises depositing a conducting material selected from the group consisting of Polysilicon, hemispherical grained (HSG) Polysilicon, Tungsten, Tungsten Nitride, Platinum, Platinum alloys, Tantalum, Ruthenium, and Ruthenium Oxides.

30. A method of forming a dielectric layer of a first thickness on a semiconductor wafer comprising:

forming the dielectric layer of the first thickness on the wafer;

positioning a shield layer on the dielectric layer;

positioning a sacrificial layer on the shield layer;

depositing conductive material on the sacrificial layer;

removing the conductive material and the sacrificial layer using a chemical mechanical polishing process adapted to remove the conductive material and the sacrificial layer wherein the shield layer is more resistant to planarization by the chemical mechanical polishing process than the sacrificial layer; and

detecting when the chemical mechanical polishing process has removed the sacrificial layer.

31. The method of Claim 30, wherein the shield layer is formed of a material having a different hardness than the sacrificial layer and wherein detecting when the chemical mechanical polishing process has removed the sacrificial layer comprises detecting the transition between when the chemical mechanical polishing process is interacting with the sacrificial layer and the shield layer.

32. The method of Claim 31, wherein the step of detecting when the chemical mechanical polishing process has removed the sacrificial layer comprises sensing the current being drawn by a motor inducing relative movement between a polishing pad and the wafer and sensing when the current drawn by the motor indicates that the pad is in contact with the shield layer.

33. The method of Claim 32, wherein forming the shield layer comprises forming a dielectric antireflective coating (DARC) layer on a BPSG dielectric layer.

34. The method of Claim 30, wherein the chemical mechanical polishing process is performed using an etchant selected to remove the sacrificial layer and wherein the shield layer is selected to be resistant to the selected etchant.

35. The method of Claim 34, wherein the shield layer is comprised of a Nitride layer positioned on the dielectric layer.

36. The method of Claim 35, wherein the sacrificial layer is comprised of a BPSG Oxide layer formed on the Nitride layer.

37. The method of Claim 30, further comprising forming a cavity in the dielectric layer and wherein depositing the conductive material on the sacrificial layer results in the cavity being filled with the conductive material.

38. An electrical structure formed using semiconductor processing techniques, the structure comprising:

a circuit node;

a layer of dielectric material formed over the circuit node to a desired thickness and having an opening formed therein;

a shield layer formed on an outer surface of the dielectric layer;

a sacrificial layer formed on an outer surface of the shield layer; and

a conductive plug formed of a conductive material positioned within the opening so as to contact the circuit node, wherein the shield layer provides a shield against thinning of the dielectric layer from the desired thickness and wherein the sacrificial layer facilitates CMP removal of excess conductive material during formation of the conductive plug.

39. The structure of Claim 38, wherein the circuit node is comprised of a semiconductor substrate.

40. The structure of Claim 38, wherein the layer of dielectric material is comprised of a layer of BPSG Oxide.

41. The structure of Claim 38, wherein the shield layer is comprised of a layer of material selected so as to define an end point for a CMP process used to remove excess conductive material during formation of the conductive plug.

42. The structure of Claim 41, wherein the shield layer is formed of a material that is less susceptible to removal by CMP than the material forming the conductive plug so that frictional engagement during the CMP process increases when the CMP process reaches the shield layer so as to thereby define an end point.

43. The structure of Claim 42, wherein the shield layer is formed of a dielectric antireflective coating (DARC).

44. The structure of Claim 42, wherein the shield layer is formed of a layer of Nitride material.

45. The structure of Claim 38, wherein the conductive material forming the conductive plug is comprised of Polysilicon material.

46. A capacitor structure formed using semiconductor processing techniques, the structure comprising:

a layer of dielectric material formed to a desired thickness and having an opening formed therein;

a shield layer formed on an outer surface of the dielectric layer; and

a bottom electrode formed of a conductive material positioned within the opening so as to be adjacent the dielectric layer, wherein the shield layer provides a shield against thinning of the dielectric layer from the desired thickness during formation of the bottom electrode;

a capacitor dielectric formed on an outer surface of the bottom electrode within the opening; and

an upper electrode formed of a conductive material on the outer surface of the capacitor dielectric.

47. The capacitor structure of Claim 46, further comprising a substrate and a contact plug that interconnects the bottom electrode to the substrate.

48. The capacitor structure of Claim 46, wherein the layer of dielectric material is comprised of a layer of BPSG Oxide.

49. The capacitor structure of Claim 46, wherein the shield layer is comprised of a layer of material selected so as to define an end point for a CMP process used to remove excess conductive material during formation of the capacitor structure.

50. The capacitor structure of Claim 49, wherein the shield layer is formed of a material that is less susceptible to removal by CMP than the material forming the capacitor structure so that frictional engagement during the CMP process increases when the CMP process reaches the shield layer so as to thereby define an end point.

51. The structure of Claim 50, wherein the shield layer is formed of a layer of Nitride material.

52. The capacitor structure of Claim 46, wherein the shield layer is formed of a dielectric antireflective coating (DARC).

53. The structure of Claim 46, wherein the bottom electrode comprises a conducting material selected from the group consisting of hemispherical grained (HSG) Polysilicon, Platinum, Platinum alloys, Tantalum, Tungsten, Tungsten Nitride, Ruthenium, and Ruthenium Oxides.

54. The structure of Claim 46, wherein the upper electrode comprises a conducting material selected from the group consisting of Polysilicon, hemispherical

grained (HSG) Polysilicon, Platinum, Platinum alloys, Tungsten, Tungsten Nitride, Ruthenium, and Ruthenium Oxides, ~~Iridium,~~ and Iridium Oxides.

55. The structure of Claim 46, wherein the capacitor dielectric comprises a high-K dielectric material selected from the group consisting of Tantalum Oxide, Aluminum Oxide and Barium Strontium Titanate.

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